# **PreciseTime**_Basic_ : IEEE1588 V2 IP Core
## Sub-microsecond Ethernet based synchronization

## General description

**PreciseTime**_Basic_ is a IEEE1588-2008 compliant clock synchronization IP core for FPGA devices. It is capable of accurately time stamp IEEE1588 telegrams and to provide a compatible timer with sub-microsecond precision.

**PreciseTime**_Basic_ maintains the clock and it is in charge of timestamping and frame analysis. Multiple Ethernet connections can share the same timer or different Ethernet connections may have their individual timer.

Standard versions are available for PLB and AXI4 on-chip buses.
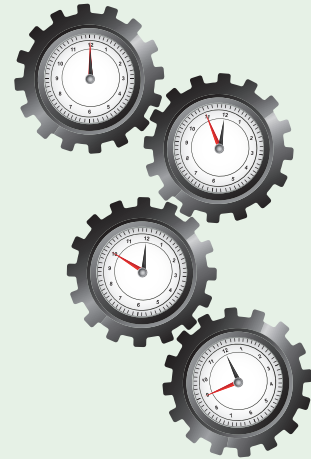
## Applications

By its implementation modularity **PreciseTime**_Basic_ may be used in a wide range of applications. Furthermore, it does not need any specific _hard_ module inside the FPGA, so it can be implemented seamless in low-cost or high-end FPGA families. Among other sectors where **PreciseTime**_Basic_ can be directly used, highlight:

- Energy and Power Electronics
- Industrial Ethernet communications
- Wireless base stations synchronization
- Wired Networks synchronization
- Home Automation
- Military and Software-Defined Radio

## Basic Package

**PreciseTime**_Basic_ basic package includes the following items:

- IP core netlist ready for seamless integration in XPS
- Software driver for easy integration with different PTP software stacks (IXXAT PTP, GPL OpenPTP)
- Reference design for SP605 Spartan-6 Evaluation Board
- Training seminar

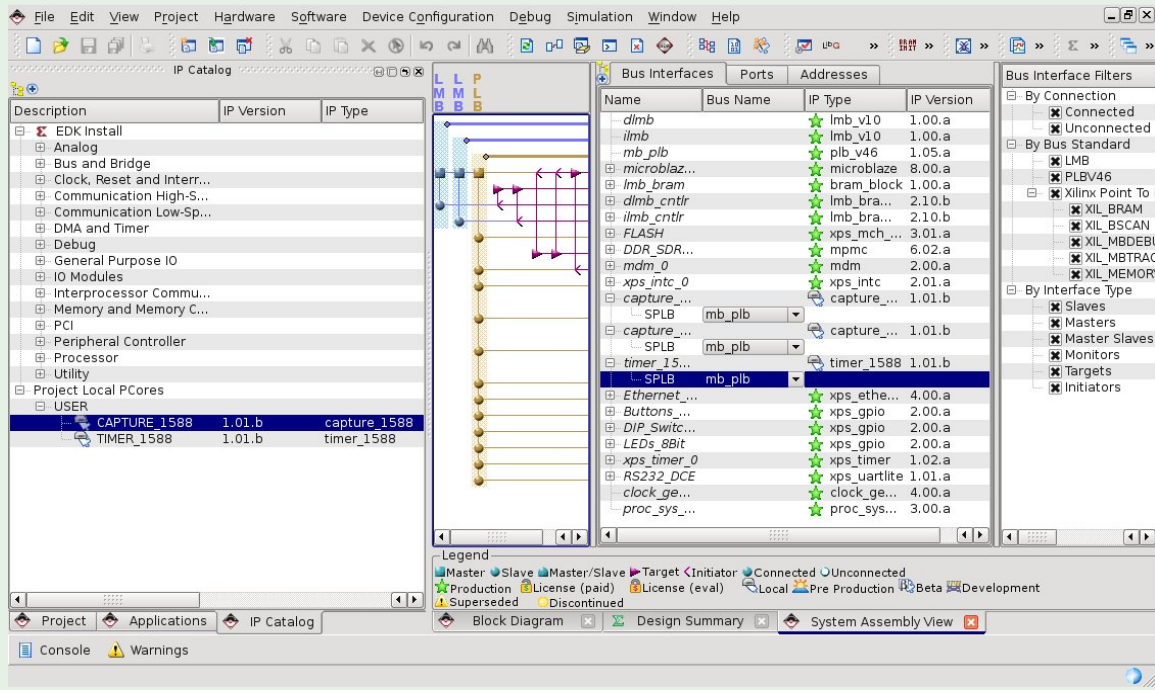**PreciseTime**_Basic_ is provided with a reference PTP software stack:

- GPL SourceForge PTPd stack
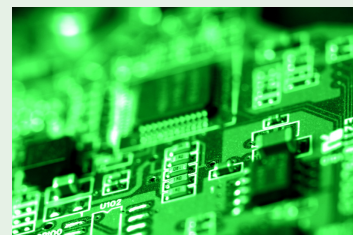
**SoC**_e_ offers the following engineering services related to this product:

- FPGA custom design (SoPC Microblaze based solution)
- Software and OS (Linux) integration
- Combination with other IPs or networking solutions
- Custom board design

# **SoC**_e_

# Integration example



# Resource utilization and accuracy

**PreciseTime**_Basic_ has been described using VHDL language to facilitate the implementation in different FPGA families and devices. The core is wrapped to be PLB compatible or AXI4 although can be customized for other on-chip Bus.

- A complete PLB implementation for one Ethernet interface (1 timer and 2 timestamping units RX/TX) needs approximately 1000 Spartan-6 Slices.
- Nanosecond timer counter grain, frequency and offset can be configured to achieve sub-microsecond synchronization. Frequency can be fine tuned down to nanoseconds per second.
- Messages are timestamped with nanosecond accuracy close to the physical layer to minimize unpredictable latencies.

# About the company

**SoC**_e_ (www.soc-e.com) offers specialized design services of FPGAs, SoPCs, IPs and embedded systems. The staff at **SoC**_e_ is formed by an interdisciplinary group of professionals with a proven experience in the design of FPGA based systems and embedded systems in general. **SoC**_e_ is involved in constant activities of R+D with cutting-edge research groups and possesses a well established net of partners and suppliers.

# Ordering information and contact

For any further question, ordering information, quotation or licensing options contact **SoC**_e_ :

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