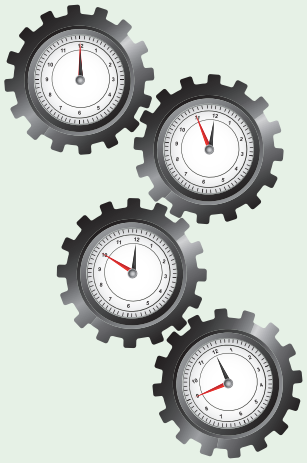
PreciseTimeBasic ZYNQ Edition: IEEE1588 V2 IP Core

Sub-microsecond Ethernet based synchronization

General description

PreciseTime*Basic* ZYNQ Ed. is a IEEE1588-2008 compliant clock synchronization IP core for FPGA devices. It is capable of accurately time stamp IEEE1588 telegrams and to provide a compatible timer with sub-microsecond precision.
PreciseTime*Basic* ZYNQ Ed. maintains the clock and it is in charge of timestamping and frame analysis. Multiple Ethernet connections can share the same timer or different Ethernet connections may have their individual timer.
The IP core has been designed to be connected to the dual ARM Cortex-9 processor present in the Zynq platform using an AXI on-chip bus.



Applications

By its implementation modularity **PreciseTime***Basic* ZYNQ Ed. may be used in a wide range of applications. Furthermore, it does not need any specific *hard* module inside the FPGA, so it can be implemented seamless in low-cost or high-end ZYNQ SoC families. Among other sectors where **PreciseTime***Basic* ZYNQ Ed. can be directly used, highlight:

- Energy and Power Electronics
- Industrial Ethernet communications
- Wireless base stations synchronization
- Wired Networks synchronization
- Home Automation
- Military and Software-Defined Radio

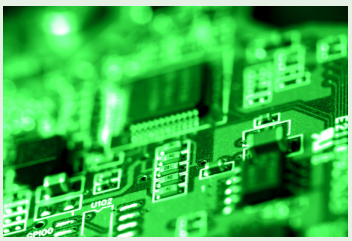
Basic Package

PreciseTime*Basic* basic package includes the following items:

- IP core netlist ready for seamless integration in XPS
- Software driver for easy integration with different PTP software stacks (IXXAT PTP, GPL OpenPTP)
- Reference design for Zynq®-7000 AP SoC ZC702 Evaluation Kit
- Training seminar

PreciseTime*Basic* is provided with a reference PTP software stack:

- GPL SourceForge PTPd stack

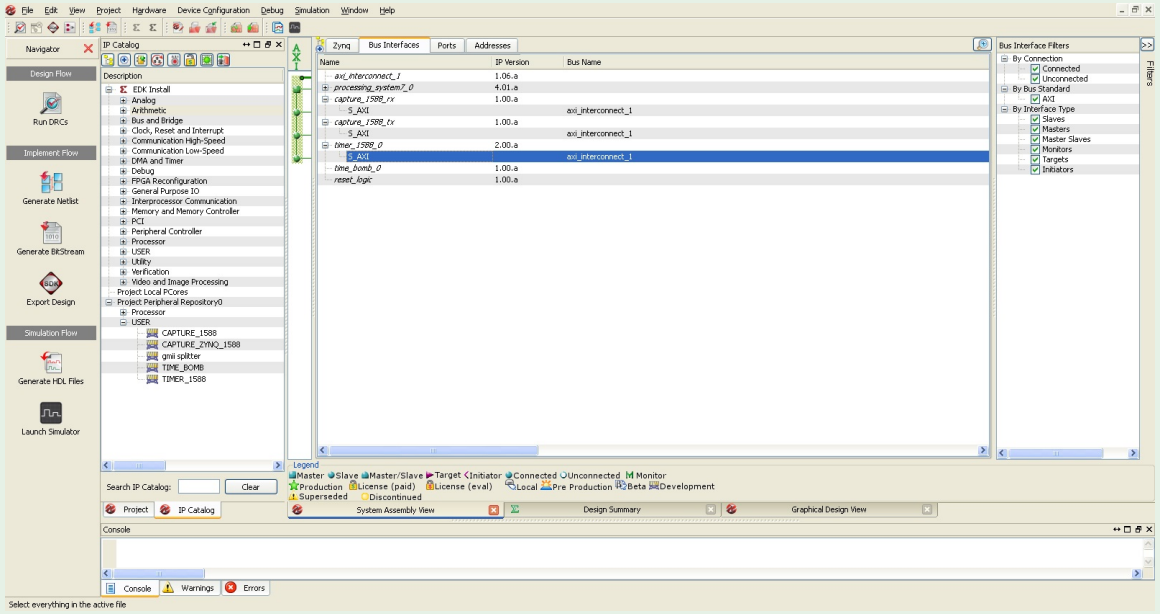


SoC*e* offers the following engineering services related to this product:

- FPGA custom design (SoPC ZYNQ based solution)
- Software and OS (Linux) integration
- Combination with other IPs or networking solutions
- Custom board design

SoC*e*

Integration example



Resource utilization and accuracy

PreciseTime*Basic* ZYNQ Ed. has been described using VHDL language to facilitate the implementation in different FPGA families and devices. The core is wrapped to be AXI compatible although can be customized for other on-chip Bus.

- A complete AXI implementation for one Ethernet interface (1 timer and 2 timestamping units RX/TX) using the ARM Cortex-A9 processor and the Gigabit Ethernet Controller that are present in the Processing System (PS) section needs approximately 1333 Slice Registers.
- Nanosecond timer counter grain, frequency and offset can be configured to achieve sub-microsecond synchronization. Frequency can be fine tuned down to nanoseconds per second.
- Messages are timestamped with nanosecond accuracy close to the physical layer to minimize unpredictable latencies.

About the company

SoC*e* (www.soc-e.com) offers specialized design services of FPGAs, SoPCs, IPs and embedded systems. The staff at **SoC***e* is formed by an interdisciplinary group of professionals with a proven experience in the design of FPGA based systems and embedded systems in general. **SoC***e* is involved in constant activities of R+D with cutting-edge research groups and possesses a well established net of partners and suppliers.

Ordering information and contact

For any further question, ordering information, quotation or licensing options contact **SoC***e* :

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