

IEC61850-9-2 PROCESS BUS IMPLEMENTATION ON IEDs

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ABSTRACT

The Process Bus implementation provides many advantages to the utilities: copper reduction-cost reduction, engineering simplification, better failure detection system, lower risk of electrical accidents, interoperability, etc. The Process Bus is based on two types of multicast messages, the GOOSE (defined in IEC61850-8-1) and the Sampled Values (SV, defined in IEC61850-9-2). After the successful implementation of the GOOSE message in the Station Bus, utilities are starting to use it in the Process Bus, together with the SV message. Pilot projects are currently in operation.

This paper focuses on the SV messages and their influence on the IEDs. Devices working with SV, coming from the Merging Units (MU) or from the non-conventional CTs (NCCT), have to cope with issues not considered with conventional IEDs: resampling, frequency tracking, counter-measures to be taken during loss or delay of SV, etc

The paper explains the issues found during the development of an IED based on SV, describing the adopted solutions. Interpolation algorithms are used for resampling and for lost SV estimation. The frequency tracking algorithm is reviewed.

Tests results for different conditions are included.

1. INTRODUCTION

These last years, thanks to the positive development of IEC 61850 inside the substation world, mainly in terms of communication between the bay level and the station level (protection relays, local HMIs, SCADA, etc.), the possibility of a direct communication between the process equipment and the bay level IEDs has experienced a great boost. In this way, an introduction of a process bus based on IEC 61850-9-2 and IEC 61850-8-1, where the voltage and current sensors transmit sampled values and the switchgear sends its information, would result in benefits for the engineering process, commissioning and future maintenance of the substation environment.

We are not just talking about the reduction of the copper wiring, what at first sight it is automatically translated into cost savings, but also about the reduction of the IEDs size, the automated testing possibilities, taking advantage of the technology, simple wiring and flexible architectures, enhancements of protection functions by giving access to any signal from the process level to any place in the bay level, and the well-known interoperability. So, instead of providing physical wired analog inputs to conventional IEDs which work with analog to digital converters, the Merging Unit device appears and the analog signals from CTs/VTs are digitalized into them.

A merging unit provides synchronized samples from the three phase currents and the three phase voltages to the communication network. In many projects where the process bus appears for the first time, conventional CTs and VTs are used, so the merging unit will just do the analogue to digital conversion of the conventional output of the CTs and VTs. In those innovative projects where non-conventional sensors like optical sensors (NCIT) take place, the merging unit will be integrated in the electronics required to process the optical signal, taking part of the NCIT itself. In both cases, the old analog values are converted into a standard data packet format called as Sampled Value (SV) and sent through the communication cable and, therefore the process bus network can carry many digital signals.

As some protection function, such as the transformer differential unit or the bus bar protection unit, have to use data provided by several MUs, they must be synchronized. The MUs may have an external time synchronization source, for example a GPS clock or IRIG-B, or could use a precision time synchronization protocol (IEEE 1588). In any case, once the MUs are synchronized, the SV frames will be sent to the bay level protection and there the corresponding IEDs will take them.

A conventional digital protection relay operates with the samples received by its own ADC. It seems easy to make the relay work with the samples received via the communication link, once an Ethernet interface is provided, however some points need to be considered:

- The sampling frequency in the conventional relay and in the MU are normally different. A change in the sampling frequency or a modification of the digital filters are the two options available.
- The sampling frequency of the MU is fixed, it does not track the network frequency, therefore a frequency tracking algorithm needs to be implemented in the IED based on SV in order to keep an appropriate operation during off-nominal frequencies.
- SVs can be lost or delayed: the IED must cope with this situation.

This paper describes the implementation carried out in an IED based on 61850-9-1LE.

2. COMMUNICATION PERFORMANCE

The engineering process of a protection and automation system inside a substation relies not only in the devices themselves but on the use of an effective communication system to link various protection, control, and monitoring devices within an electric power substation. The major challenge faced by substation automation design engineers is to provide interoperability among the protection, control, and monitoring devices from the various manufacturers. The IEC61850 international standard for communications in substations brings the possibility of changing from IEC 60870-5-103 [1], MODBUS [2], DNP 3.0 [3], or other proprietary protocols to just one which provides the interoperability by defining the communication protocol, data format and the configuration language. It affects not only the design of the substation secondary circuits due to the fact that IEC61850-9-2 [4] is the part of the standard that proposes a digital link between the bay level and the process level in such way that all data is transferred in an Ethernet based communication network.

The analogue inputs that are usually hardwired to conventional IEDs, which integrate analog to digital converters and binary inputs-outputs, are replaced by an Ethernet message sent by a device called as merging unit which is located near the switchyard and connected to the instrument transformers, see figure 1. The merging unit is the centerpiece of the process bus whose main purpose is reducing the labor cost and complexity of the copper wiring between switchyard and control room, so that all the analog values are converted to digital signals, merged into a standard data frame format and sent to the process bus network by these devices. A specialization of the IEC 61850-9-2, known as IEC 61850-9-2 LE, has been created by major suppliers in order to define some of the parameters and facilitate interoperability. Nowadays, as TC57WG10 has informed anything related to the bus process is going to be located inside IEC 61869-9 [5].

savPdu 60	L (727 919)								
noASDU	80	L (1)	8	1					
Sequence of ASDU	A2	1	(720!	912)					
Sequence ASDI 1			30	L (88112)					
svID				2 (00		80		values	
empCnt							L		
confPou						82	L	values	
smnSynch						83	L	1	
Shipoynon Convenee of Date						85	L	values	
Sequence of Data					Ξ	87	L		
					SU				values
					A				values
								Data	values
								Set	values
									values
									values
									values
Sequence ASDU2			30	L					
							ADSU	2	
Sequence ASDU3			30	L					
				(ADSU 3				
ASN.1 Tag L = Length]								

Figure 1. APDU of IEC 61850-9-2 sampled value message

Taking into account all the benefits the process bus provides, the IEC 61850 network has become a combination of many types of network traffic like Raw Ethernet, MMS/TCP, SNTP, IEEE 1588, TFTP, FTP, RSTP, SNMP, and other Ethernet based protocols, what means that the amount and kind of traffic the substation network must arrange is increasing more and more. So traffic problems can appear and therefore SV frames could be lost, what makes important thinking about algorithms to be used for lost SV estimation. While client-server MMS services are IP based traffic over TCP, where a delay of 100-500ms in measurements, events and status indications is accepted and the reports are unsolicited (buffered reports) or periodic (unbuffered reports), GOOSE and SV are encapsulated directly in the Ethernet layer as high priority and critical frames, see figure 2. However this elimination of TCP/IP layer reduces the reliability of packet communication. This issue has been solved in the case of the GOOSE because it is an event triggered message that is transmitted repeatedly through the network, but sampled value packets are time triggered synchronous and unsolicited frames that are transmitted at the rate of sampling frequency just once, so the analysis of packet delay and loss of SV frames is very important.



Figure 2. Message communication OSI -7 layer stack of IEC 61850

Looking at the present and the way this technology is being used inside a substation, Figure 3 shows a typical 138/34,5 kV distribution substation considered for the analysis, where two high voltage positions, a transformer and two medium voltage cabinets come into play.



Figure 3. Substation considered for the analysis

In the scenario proposed for the tests, the IEDs will be located in panels and cabinets inside a room and will communicate in a bay level ring, while the MUs will be outside, next to the instrument transformers, and taking part of a process ring. The connection between the devices and the switches is done with Fast Ethernet (100Mbps), and the connection between the switches is multimode fiber optic GbE (1000Mbps), as can be shown in figure 4.

Using this kind of topology, on the one hand the IEDs will be sending GOOSE messages between themselves and reports to the SCADA client (bay level), on the other hand we will have the MUs sending small multicast frames, with the current and voltage values they are metering, each 250µs in a 50Hz grid (80 samples per cycle) generating for example frames of 124 bytes, see figure 5, and all that traffic is flowing together through the bay level ring.



Figure 4. Network

14 0.001538	DimatSA_02:9e:a2	Iec-Tc57_04:00:01	0x88ba	IEC 61850/SV	(Sampled Value	Transmission	
15 0.001752	JkMicros_c2:7a:a4	Iec-Tc57_04:58:02	0×88ba	IEC 61850/SV	(Sampled Value	Transmission	
16 0.001787	DimatSA_02:9e:a2	Iec-Tc57_04:00:01	0x88ba	IEC 61850/SV	(Sampled Value	Transmission	
17 0.002002	JkMicros_c2:7a:a4	Iec-Tc57_04:58:02	0x88ba	IEC 61850/SV	(Sampled Value	Transmission	
18 0.002046	DimatSA_02:9e:a2	Iec-Tc57_04:00:01	0×88ba	IEC 61850/SV	(Sampled Value	Transmission	
	, 124 bytes captured)						
🖃 Ethernet II, Src: DimatSA_O	2:9e:a2 (00:e0:ab:02:9e:a	2), Dst: Iec-Tc57_04:0	0:01 (01:0	c:cd:04:00:01)	l i i i i i i i i i i i i i i i i i i i		
Destination: Iec-Tc57_04:	00:01 (01:0c:cd:04:00:01)						
Address: Iec-Tc57_04:00	:01 (01:0c:cd:04:00:01)						
1	= IG bit: Group add	dress (multicast/broad	cast)				
0	- LG bit: Globally	unique address (facto	rv default	2			
- Source: DimotsA 03:00:03	(00:00:0b:03:00:03)	unique address (racco	iy deradit)			
E Source: DimatSA_02:90:42	(00:e0:ab:02:9e:a2)						
Address: DimatSA_02:9e:	a2 (00:e0:ab:02:9e:a2)						
0 = IG bit: Individual address (unicast)							
0	= LG bit: Globally	unique address (facto	ry default)			
Type: IEC 61850/SV (Samp]	ed Value Transmission (0x)	88ba)					
Data (110 hytes)							
Data: 40000840000000607	A800101A275307380224D555E	4952					
Data 40000080000000000000000000000000000000							
[reudiu: Tro]							
0000 01 0c cd 04 00 01 00 e0	ab 02 9e a2 88 ba 40 00						
0010 00 84 00 00 00 00 60 7a	80 01 01 a2 75 30 73 80	`zu0s.					
0020 22 4d 55 5f 49 52 56 5f	5a 49 56 32 5f 82 02 08	"MU_IRV_ ZIV2					
0030 30 83 04 00 00 00 01 85	01 00 87 40 ff ff c8 1c	<@					
0040 00 00 00 00 tt te d0 77	00 00 00 00 00 01 66 64	kj					
0050 00 00 00 00 00 00 00 00	00 00 00 00 TT 8T EI 53	s					
0070 00 00 00 00 00 ff b0 11 e2	00 00 00 00 00 10 17 18	W×					
2010 00 00 00 00 11 D0 II E2	00 00 00 00						

Figure 5. Sampled Value traffic

In a normal situation, this is, with no frames in the queues of the switches, the queue of the "BUS-LINK" switch from where all the SV are going to cross, becomes the bottleneck. In this situation the frames will be delayed just by the time the switch takes to transport the data through one port to another one (it is called as switch fabric latency and in our case is $4.5 \ \mu$ s) and the time lost in the fiber optic wire. Let's consider that all the MUs are duly synchronized so the SV traffic will be generated at the same time. Not only the switch where the MUs are connected must be taken into account but also the amount of traffic that will arrive to each switch at the same time and that it will have to manage.

Making a test just with SV in the network, we can study the delays in an ideal situation, the best case. The differential transformer IED located in the switch called as "TRANSFORMER" needs the current meterings from the high voltage and the low voltage side, which are going to be sent by MU-4 and MU-6. As the MU-6 frames must cross one more switch, they will arrive to the IED with some delay:

LMU6 (124 byte frame)= [992* 1 / 100Mbps + 4.5 µs] + [992* 3 / 1000Mbps + 4.5 µs] + [992* 6 / 1000Mbps+ 4.5 µs]*2 + 992* 1 / 100Mbps = 52.7203 µs

LMU4 (124 byte frame) = [992* 1 / 100Mbps + 4.5 μ s] + [992* 3 / 1000Mbps + 4.5 μ s]*4 + 992* 1 / 100Mbps = 54.244 μ s

Due to the fact that the SVs of MU4 are going to arrive later to the "BUS-LINK" switch, it could happen that while the SVs of MU6 have already been sent, the link with the "SCADA" switch is lost and the SVs of the MU4 must travel by a longer way. In this case:

LMU4 (124 byte frame) = [992* 1 / 100Mbps + 4.5 μ s] + [992* 3 / 1000Mbps + 4.5 μ s]*7 + 992* 1 / 100Mbps = 76.672 μ s

We can see that in both situations, we have a delay lower than 250 µs. While working with mixed network traffic, although SV and GOOSE messages are protected by being market as critical network traffic with a higher priority than other traffic, in the worst case, a high-priority SV frame could be delayed not only by other frames in its own queue, but also by one full-size frame in the low priority queue that has begun transmission from the low-priority queue just ahead of the reception of the SV frames in the high-priority queue. In this new scenario, the SVs of MU6 could be sent with no problem, but the SVs of MU4 could be delayed by a lower priority frame of for example 1538 bytes (a really big one).

LMU4 (124 byte frame + 1538 byte) = $[992^* 1 / 100Mbps + 4.5 \mu s] + [992^* 3 / 1000Mbps + 4.5 \mu s]^*2 + [(992^*3+12304) / 1000Mbps + 4.5 \mu s]^*2 + 992^* 1 / 100Mbps = 78.852 \mu s$

And taken into account the other case, when the link with the "SCADA" switch is lost, this is, the worst case:

LMU4 (124 byte frame + 1538 byte) = $[992^* 1 / 100Mbps + 4.5 \mu s] + [992^* 3 / 1000Mbps + 4.5 \mu s]^*2 + [(992^*3+12304) / 1000Mbps + 4.5 \mu s]^*5 + 992^* 1 / 100Mbps = 138.192 \mu s$

So, working with this topology, the IEDs that are receiving and processing SV data would need to be able to tolerate data delayed by as much as 138.192 μ s with a jitter of 85.4717 μ s. With other kind of topologies the delay could be higher.

In the calculation done before the MUs were supposed to send the SV exactly at the same time. This assumption is not true and depending on processing time different MU can have different delays in sending the SVs. This delay difference should be added to the delay difference due to the network itself. The IEC61869 standard specifies a maximum time delay of 1.5 ms for a MU used for protection.

Apart from the delays, which are always going to be present, data lost can also happen because of traffic saturation in the network [6], where the bit error rate (BER) of the network comes also into play, but a detailed analysis of the network could avoid data lost greatly. Accordingly we could make some changes in the topology network presented, for example connecting the SV switches (SV-1, SV-2, SV-3) in star and adding links for ensure different ways from where the traffic can flow, so that we can improve the reliable operation of the devices.

3. IED IMPLEMENTATION

3.1 Sampled Value time alignment

An IED must receive the SV of the currents and voltages required to perform all the protection functions included. These currents and voltages may be measured by several MU. Typical scenarios are:

- Winding phase currents required for a transformer differential function: one MU per each winding.
- Line and bus phase voltages for a synchrocheck function: one MU to measure the line voltage/s and another MU to measure the bus voltage/s.
- Line phase currents and ground parallel line current for a distance function (with mutual coupling compensation): one MU to measure the line currents and another one to measure the parallel line current.
- Line phase voltages and two sets of phase currents for a distance function (or any function based on line voltage and current: directional overcurrent, voltage-restrained overcurrent, power directional, etc) in breaker and a half substations: one MU measuring the two sets of phase currents and another MU measuring the phase voltages or one MU measuring one set of phase currents and the phase voltages and the other one measuring the second set of phase currents.

The SV received from different MU must be synchronized with a very high accuracy (1 us or better). For high accuracy applications the substation clock, normally a GPS time reference clock, can be distributed with one of the following methods: IRIG-B (to achieve the required accuracy a modified Manchester modulation is recommended), 1 PPS (although it does not contain time information it is valid for MU synchronization as this process does not require an absolute time) or IEEE1588. The most common method used nowadays is the 1 PPS.

For protection purposes the MU will have a sampling frequency of 80 samples / cycle which means 4000 samples per second for 50 Hz and 4800 samples per second for 60 Hz. The reception of the PPS signal will force the capture of the sample number 0. The rest of the samples are captured based on the MU internal clock (considering a time between samples of 250 us for 50 Hz and 208.3 us for 60 Hz) until the next PPS is received. The drift between the MU internal clock and the GPS clock is compensated every second. All the SV will have a sequence number called Sample Counter (smpCnt). This sequence

number will be used in the IED receiving the SV to make the time alignment. The Sample Counter will go from 0 to 3999 when the rated frequency is 50 Hz and from 0 to 4799 when the rated frequency is 60 Hz.

SV received from different MU may not arrive at the same time as it was explained in point 3. This will depend on the substation architecture and on the MU processing time. A time delay between the first and the last SV frame received should be considered. If a SV frame arrives later than this time delay the SV will be considered lost. In the architecture explained in the former section a time delay of 85.4717 μ s, due to the network itself, was calculated. By also considering the processing time of the MU, a typical time delay could be around 2 ms.

3.2 Sampling Frequency Change

When a conventional IED is converted into an IED based on SV two options can be used as far as the metering module is concerned:

- Adapt the filters to work with the new sampling frequency.
- Change the sampling frequency with a resampling algorithm and use the same filters.

The second option was chosen as the preferred one because the resampling algorithm was also required for the frequency tracking (see next point) and the change in the relay functionality was considered much lower than in the first case, reducing the risk of errors. The tests, in this case, were mainly focused on the resampling algorithm. The conventional relays transformed into IEC61850-9-2LE relays had a sampling rate of 32 samples / cycle. For the oscillography module the samples received from the MU were used (with a sampling rate of 80 samples / cycle).

The resampling algorithm will be described in the next point.

3.3 Frequency Tracking

The sampling rate of the MU is fixed, it does not change with the frequency: 80 samples per 50 / 60 Hz cycle. If the samples received from the MU are directly used for protection purposes errors during offnominal frequencies will appear. Reference [7] describes a frequency tracking algorithm that modifies the time between samples, based on the frequency measurement, to make the Discrete Fourier Transform (DFT) window span exactly one cycle. The frequency was measured based on hardware zero-crossings using a hardware low pass filter. In the IEC61850-9-2LE relay the frequency is measured based on software zero-crossings using the raw samples received from the MU (with a sampling frequency of 80 samples per cycle). A digital low pass filter was implemented. The same method described in [7] for filtering phase-shifts, based on several zero-crossings and on the sign of the frequency change, was considered in the SV based relay. In order to consider the three-phases for the frequency calculation the α Clark transformation was used.

With the aim of obtaining 32 samples spanning exactly one cycle a resampling algorithm based on a third order polynomial interpolation was implemented. In order to reduce the computational load of the microprocessors a Newton polynomial based on the Divided Differences was selected due to its recursive implementation.

The third order Newton polynomial is:

 $P_3(x) = f(t_0) + f[t_0, t_1] \cdot (t - t_0) + f[t_0, t_1, t_2] \cdot (t - t_0) \cdot (t - t_1) + f[t_0, t_1, t_2, t_3] \cdot (t - t_0) \cdot (t - t_1) \cdot (t - t_2)$ where:

 $f(t_i)$ is a zero-order divided difference

 $f[t_i, t_{i-1}] = \frac{f(t_i) - f(t_{i-1})}{t_i - t_{i-1}}$ is a first-order divided difference

 $f[t_{i}, t_{i-1}, t_{i-2}] = \frac{f[t_{i-1}, t_{i}] - f[t_{i-2}, t_{i-1}]}{t_{i} - t_{i-2}}$ is a second-order divided difference

$$f[t_{i-3}, t_{i-2}, t_{i-1}, t_i] = \frac{f[t_{i-2}, t_{i-1}, t_i] - f[t_{i-3}, t_{i-2}, t_{i-1}]}{t_i - t_{i-3}}$$
 is a third-order divided difference

The value $t_i - t_{i-1}$ is constant:

For frated=50 Hz: $t_i - t_{i-1} = 250 \ us$

For frated=60 Hz: $t_i - t_{i-1} = 208.3 \text{ us}$

t is the time for the sample to be calculated; this time will be obtained from the frequency measurement.

Given the low time between the samples received from the MU, the algorithm will have a very high accuracy. Tests are described in point 4.5.

3.4 Estimation of lost SV

Most of the relays include functions working with phasors: magnitude and angle. Phasors are normally obtained with digital filtering using several samples spanned in a window time which can vary from fractions of a cycle up to several cycles depending on the application. The calculation window slides the time between samples when a new sample is received. The most common used digital filtering is the Discrete Fourier Transform (DFT) using sliding windows of one cycle. The loss of a sample will affect the phasor calculation for the duration of the filtering window. It is not until the window has slid its duration that the lost sample gets out of it.

The effect of the loss of one or more samples depends on the method used to fill the gaps created in the sample buffer: zeros, the value of the last sample, the value of the new samples, etc. Figure 6 shows a sinusoidal voltage wave in which five consecutive samples have been lost. The wave with circles (V1) does not lose any sample. In the wave with crosses (V2) the lost samples were replaced by zeros; in the wave with squares (V3) the lost samples were replaced by the value of the last sample; in the wave with triangles (V4) the lost samples were replaced with the new samples that arrive after the last lost sample. The magnitude and angle for the four waveforms are shown in figures 7 and 8. With regard to V1 magnitude. V2 magnitude is lower, V3 magnitude is higher and V4 magnitude oscillates around V1 magnitude. After 80 samples from the last lost sample V1, V2, V3 and V4 magnitudes are all the same. With regard to V1 angle, V2 angle is higher, V3 angle is lower and V4 angle oscillates with higher values. Note that after the 80 samples from the last lost sample V4 angle does not return to its original value. That is why the method used for the wave V4 should be avoided. New samples should always fill their correct position based on the sample counter mentioned in point 4.1.

Due to the errors in the phasor calculation generated by the lost samples a blocking could be applied to the affected protection functions. This blocking should start when the first sample is lost and finish one cycle after the last lost sample. If the samples are lost during the start of a fault the operation of the protection will be delayed one-cycle. In order to avoid this delay an algorithm to estimate lost samples is implemented. The algorithm will use the same polynomial interpolation described in the former point.

A sample will be considered lost if:

- It is delayed more than the time delay considered in point 4.1
- Its quality is invalid
- Its sample synchronized flag is FALSE



Figure 6. Different treatments for the lost samples



Figure 7. Magnitudes for the voltage waveforms of figure 6



Figure 8. Angles for the voltage waveforms of figure 6

NOTE: When the protection functions are solely based on samples, not on the DFT calculation, the effect of lost SV will be less important and a blocking could be applied just during the time the SV are lost.

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3.5 Tests

3.5.1 Resampling algorithm

Figure 9 shows a sinusoidal voltage waveform with the rated RMS value and 51 Hz. The waveform is sampled with 80 samples per 50 Hz cycle (samples represented with circles), with 32 samples per 51 Hz cycle (samples represented by crosses) and with 32 samples per 51 Hz cycle calculated with the polynomial interpolation (samples represented by squares). As it can be seen the direct sampling (crosses) and the resampling (squares) give exactly the same results.

A comparison between first, second and third order Newton polynomials was done for a 50 Hz waveform. The differences for the negative half cycle of the wave can be observed in figure 10. The absolute and relative errors, for each sample, are shown in figures 11 and 12 respectively. The errors for the second and third polynomial are practically null. The error of -3.29% in the third polynomial coincides with a zero-crossing, being the absolute error negligible (3.93×10^{-16}) .



Figure 9. Sampled 51 Hz voltage waveform at 80 samples per 50 Hz cycle (circles), at 32 samples per 51 Hz cycle, directly (crosses) and via resampling (squares)



Figure 10. Sampled 50 Hz voltage waveform at 32 samples per 50 Hz cycle, directly (circles) and via resampling with polynomial of 3rd order (crosses), 2nd order (squares) and 1st order (triangles)



Figure 11. Absolute errors for polynomials of 3rd order (circles), 2nd order (crosses) and 1st order (squares)



Figure 12. Relative errors for polynomials of 3rd order (circles), 2nd order (crosses) and 1st order (squares)

Influence of the harmonics

Harmonics from second to tenth were tested considering a 20% THD. The error in the RMS value calculation is included in the following table for 1st order, 2nd order and 3rd order polynomials. As it can be seen the error for the 3rd order polynomial is negligible.

HARMONIC	ERROR FOR POLYNOMIAL INTERPOLATION (%)					
	3rd order 2nd order		1st order			
2	7,41E-05	-4,70E-03	0,897			
3	7,41E-05	-6,84E-03	1,126			
4	7,41E-05	0,039	0,867			
5	7,41E-05	-0,027	0,823			
6	7,41E-05	0,019	0,958			
7	7,41E-05	-0,089	0,815			
8	7,41E-05	-0,022	1,609			
9	7,40E-05	0,206	0,503			
10	7,40E-05	-0,092	1,075			

Table 1. Influence of the harmonics on the resampling process

Influence of DC offset

The error with DC offset for different time constants is negligible both for 2nd and 3rd order polynomials.

3.5.2 Estimation of lost SV

Sinusoidal waveforms

Tests with up to 10 consecutive lost samples were performed. If the samples of the waveform V1 (shown in figure 12) between points A and B are lost, they can be estimated with polynomials of first order (VP1), second order (VP2) and third order (VP3).



Figure 12. Original voltage waveform (V1) and voltage waveform with the ten lost samples (from A to B) estimated with polynomials of 1st order (VP1), 2nd order (VP2) and 3rd order (VP3)

The error in the voltage magnitude calculated with each polynomial is -1.613%, -0.063% and -0.044% for the first order, second order and third order, respectively. If the ten samples are lost in another point of the waveform (see figure 13) the results will be different. The errors will be -0.022%, -0.0086%, -0.0061% for the first order, second order and third order polynomials, respectively. Sweeping all the points in the waveform, the maximum error for the first, second and third order polynomials is -1.633%, 0.045% and -0.163%, respectively.



Figure 13. Original voltage waveform (V1) and voltage waveform with the ten lost samples (from A to B) estimated with polynomials of 1st order (VP1), 2nd order (VP2) and 3rd order (VP3)

Influence of harmonics

Tests up to the tenth harmonic were done. If ten consecutive lost samples were considered, the maximum errors (in certain points of the waveform) exceeded 5%. Tests with five consecutive lost samples were therefore performed. RMS errors are shown in table 2.

HARMONIC	ERROR FOR POLYNOMIAL INTERPOLATION (%)						
	3rd order	2nd order	1st order				
2	1,20E-02	0,047	-0,457				
3	4,00E-02	-0,99	-0,641				
4	1,15E-01	-0,245	-0,952				
5	0,035	-0,516	-0,94				
6	-0,526	0,848	-1,433				
7	-0,969	0,956	-2,226				
8	-1,326	-1,863	-0,738				
9	1,917	-1,659	-2,886				
10	3,522	3,097	-2,604				

Table 2. Influence of the harmonics on the estimation of lost samples

Influence of DC offset

The addition of DC offset does not, appreciably, affect the error in the polynomial estimation.

3.5.3 Tests of protection units during adverse conditions

A transformer differential relay was tested forcing the loss of 5 Sampled Values each half-cycle in the currents of the first winding. The results for the search test of the differential characteristic are shown in figure 14. As it can be seen the test was passed correctly.



Figure 14. Differential characteristic search test with 5 SV lost per half-cycle

An oscillo from one of the injections was recorded during the test. As it can be observed in figure 15, the currents in the first winding (IW1A, IW1B and IW1C) are perfect sinusoidals and no lost sample is seen. This is because the lost samples were already estimated. Below the currents of both windings, there is a lost sample counter (LOSS_SV). It can be checked that the counter increases 5 samples every half-cycle. The period between lost samples was chosen a little bit lower than half-cycle, 38 samples, in order to force the loss of samples occuring at different points of the waveform during the test.



Figure 15. Oscillo taken from the differential characteristic search test with 5 SV lost per half-cycle



A test for the harmonic blocking unit was also performed. The results can be shown in figure 16.

Figure 16. Harmonic blocking test with 5 SV lost per half-cycle

An external fault with CT saturation was also simulated forcing the loss of 5 SV per half-cycle. The oscillo recorded can be seen in figure 17. The external fault detector [8] operated correctly, blocking the differential unit. The signals activated were:

EXT_CDIR_PS: External fault by positive-sequence directional comparison unit

EXT_CDIR_A: External fault by phase A directional comparison unit

EXT_CDIR_B: External fault by phase B directional comparison unit

EXT_CDIR_C: External fault by phase C directional comparison unit

EXT_DIFI_A: External fault by phase A differential unit based on instantaneous values

EXT_DIFI_B: External fault by phase B differential unit based on instantaneous values

EXT_DIFI_A: External fault by phase C differential unit based on instantaneous values



Figure 17. Oscillo for an external fault with CT saturation with 5 SV lost per half-cycle

3. REAL INSTALLATION

Process Bus IEDs were installed in Benavente substation, 132 kV, owned by Iberdrola, an Spanish distribution company. The communication architecture is shown in figure 18. ZIV installed the following IEDs: feeder, transformer differential and distance protections. It also installed a MU and a RIO (remote input-output) module. As the Process Bus system was built in parallel with a conventional Protection and Control system a comparison between oscillos recorded by the conventional and the Process Bus IEDs was possible. Figure 19 shows the oscillos recorded by the conventional distance relay, the Process Bus distance IED (subscribed to the ZIV MU) and the Process Bus feeder IED (subscribed to the Arteche Optical CT) for a fault on one of the lines. As it can be checked the waveforms are practically identical.



Figure 18. Communication arquitecture for the Process Bus system in 132 kV Benavente substation



Figure 19. Oscillo recorded from the conventional distance IED (red - Ia1), the Process Bus distance IED (Ia2 - blue) and the Process Bus feeder IED (Ia3 - green) for a fault in one of the lines

4. CONCLUSION

This paper has described the key points that affect the conversion of a conventional IED into an IED based on SV:

SV alignment: when the IED is subscribed to several MU a time delay between the SV coming from the different MU should be considered. This time delay depends on the communications architecture and the MU processing time. A time delay of 2 ms was considered in the design.

Sampling frequency change: the change from the MU sampling frequency to the sampling frequency of the conventional IED was implemented in order to maintain the digital filters of the conventional relay. The resampling was done by means of a third order Newton polynomial interpolation based on the Divided Differences. Tests have shown very good performance in the presence of harmonics and DC offset.

Frequency tracking: the sampling frequency of the MU must be changed to track the network frequency. A frequency tracking algorithm based on a zero-crossing detector and the resampling method described was implemented.

Estimation of lost samples: the implemented algorithm uses the same polynomial interpolation applied for resampling. The algorithm tolerates, with high accuracy, the loss of ten consecutive SV when sinusoidal waveforms are considered, however it reduces its accuracy in the presence of high order harmonics. An adequate accuracy is achieved for the loss of up to five consecutive samples.

Tests on IEDs including the described algorithms have been performed showing good results. The IEDs have been installed in a real substation.

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BIOGRAPHIES

Roberto Cimadevilla graduated in Electrical Engineering from the Superior Engineering College of Gijón, Spain in 2001. He later obtained a master's degree in "Analysis, simulation and management of electrical power systems" from the University of País Vasco, Spain. He previously worked for Red Eléctrica de España (REE – Spanish TSO) as a Protection Relay Engineer. Roberto joined ZIV in 2003 as an Application Engineer, being responsible in this area for the development of a new distance relay, a new transformer differential relay, a phasor measurement unit and a line differential relay. From 2011 to 2013 Roberto worked as the Manager of the Application Engineering Department. He is now the Technical Manager of the Grid Automation Division. Roberto has written several technical papers, most of them presented at international conferences. Roberto has also participated in some CIGRE B5 working groups. He is currently a regular member of B5.48 working group.

Iñigo Ferrero graduated in Automatic and Electronic Engineering from the Superior Engineering College of Deusto, Spain in 2005. He previously worked for Ikerlan as I+D+I Engineer. Iñigo joined ZIV in 2007 as a Control Engineer, becoming later on the Manager of the Control Department. He then moved to the Application Engineering Department, being responsible in this area for the development of new IEC61850 features. Íñigo is currently working as the Manager of the Application Engineering Department.

José Miguel Yarza received his M.S. degree on Electrical Engineering from Basque Country University. He later obtained a Master Degree on "Quality and Security in electrical energy delivery. Power system protections" from the same University, and a MBA from ESEUNE Business School in 2008. He joined ZIV in 1996 where he held several positions, including Application and Technical Manager of ZIV GRID AUTOMATION. He is presently the R&D Manager of the CG AUTOMATION BU. He is a member of AENOR SC57 (Spanish standardization body), IEC TC57 WG10 and several CIGRÉ working groups.